David Sarnoff Research Center
Subsidiary of SRI International

CERAMIC/METAL COMPOSITE CIRCUIT-BOARD-LEVEL TECHNOLOGY FOR APPLICATION SPECIFIC ELECTRONIC MODULES (ASEMs)

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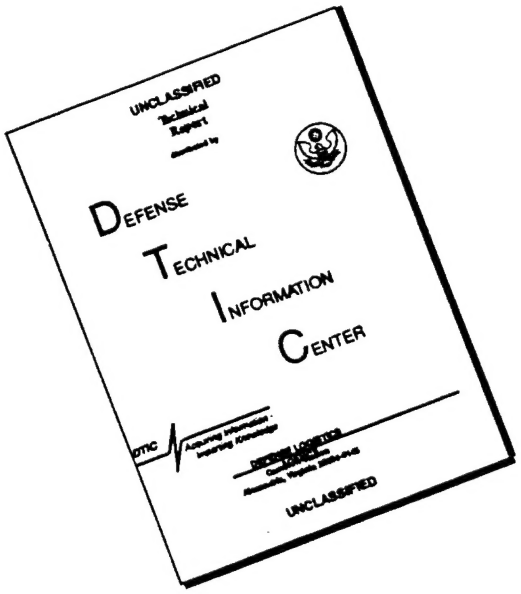

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Member Technical Staff, Electronic Packaging

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Section I
WBS Task 2.1: Technology Transfer to Merchant Suppliers

A. TASK OBJECTIVE

Transfer the LTCC-M technology to a merchant circuit supplier, Dielectric Laboratories Inc. (DLI). This task will require a steady supply of several custom glasses that were developed during the Phase 1 program. One or more glass producers will be qualified to supply materials to the David Sarnoff Research Center or its designee to produce LTCC-M circuit boards and packages. The Phase 1 technology will be interactively transferred to DLI, who will be qualified by the fabrication of test structures and technology demonstration modules. During this transfer DLI will faithfully reproduce the LTCC-M processes that have been already implemented at Sarnoff.

B. INTRODUCTION

In July, 1995 a Technology Transfer program was begun between Sarnoff and Alcoa Electronic Packaging Inc. However, on December 21, 1995 Alcoa announced its intention to exit the ceramic packaging business. In the ensuing months the effort with Alcoa was wound down, and Dielectric Laboratories Inc. was identified as a company qualified to accept an LTCC-M technology transfer and become a merchant supplier of LTCC-M packages and substrates to commercial and military end-users. This ASEM contract was modified on July 16, 1996 to begin the Technology Transfer to Dielectric Laboratories Inc. Based on comments from the Technology Transfer to Alcoa, a number of improvements in materials and processes have been incorporated into the transfer to DLI. These include a greatly simplified Cu/Mo/Cu contact process using a silver thick film ink MC-6, and an improved via ink that produces lower via bumps.

C. TECHNOLOGY TRANSFER TO DIELECTRIC LABORATORIES INC.

Technology Transfer Training

Technology Training sessions were held at the David Sarnoff Research Center with DLI personnel receiving instruction, detailed handouts, and hands-on training with Sarnoff equipment. These training sessions covered all areas of the LTCC-M technology required for fabrication of the C-band Power Amplifier Technology Demonstration Module. Covered in these sessions were:

- Plating of Cu/Mo/Cu
- Glazing
- Green tape slurry preparation and tape casting
- Custom glass preparation
- Thick film ink formulations and screen printing
- Cu/Mo/Cu contact formation
- Firing profiles
- Top conductor plating.

Samples were prepared for use at DLI in setting up their equipment.

Outside Sourcing

DLI has decided to purchase tape casting services from Richard E. Mistler, Inc., (Morrisville, PA) and thick film ink preparation services from Hereaus Cermalloy (Conshohocken, PA). All glasses and metal powders will be provided by DLI.

Materials

- All materials have been received except for the glasses from Sem-Com. They were due August 21 but are now due to ship on September 4, 1996 instead of August 21.
- The thick film inks were prepared by Cermalloy, and both Sarnoff and DLI personnel went to Cermalloy to discuss the materials and process issues. Cermalloy found that the organic binders were no problem although some of the resulting ink viscosities were different than Sarnoff values. (This difference could be due to the fact that Sarnoff measures viscosity at 100 rpm and Cermalloy measures viscosity at 10 rpm.). The final inks were also visually good. We did see some color variation between the Sarnoff and Cermalloy inks which was attributed to contamination from the stainless steel rollers. Cermalloy made two lots from the same raw materials.
- The first development tape lot was received from Mistler (DLI-Lot 1X). The thickness was twice what it should be. We also saw a discoloration on the surface that is probably due to the fish oil. When the tape was laminated at DLI, twice the pressure was needed to make the sheets stick together. Sarnoff was able to laminate the Mistler tape at the correct pressure. We believe that the difference may be due to the heating of the lamination plates. A second experimental lot of tape (lot 2X) was cast at Mistler and the thickness was very close to target.
- A second lot of Cu/Mo/Cu metal core in 0.010" and 0.020" thicknesses were ordered.

Equipment/Processes

- The furnace is connected and profiles are being established.
- The glazing and oxidation profiles have been established. A part from Sarnoff was oxidized at DLI and sent back to Sarnoff for evaluation. Except for some slight evidence of insufficient cleaning, the results were good.
- A sample of BX-141SC glaze was squeegeed onto a Sarnoff oxidized sample and fired using the glazing profile. The result was acceptable, keeping in mind that the glaze was not printed. We now have a printed sample from Sarnoff that we will fire in this profile as soon as the firing profile qualification is done.
- DLI has made artwork for both the glaze and the LN-1 patterns and have received back photoplots. Screens have been ordered.
- The DLI furnace firing profile has taken longer than expected to establish. The slow belt speed is causing the front end of the furnace to excessively heat up. DLI has been in consultation with Lindbergh about the problem and is now in the process of adjusting the furnace controllers for zones 1, 2, 3, 4, and 5 to obtain better control.

- The DLI plating line is up and running, parts have been successfully cleaned and plated. In order to save on Cu/Mo/Cu cores, DLI is establishing the process on copper sheets.
- The AMI printer is being retrofitted, and remains on schedule at this time.
- DLI is retrofitting a lamination press with a low pressure digital gauge and pressure cell for use on this program

Tooling

- The tooling required for this program is on order. This includes a blanking die, lamination plates and a punch and die specific to the Raytheon C-Band amplifier. In addition, DLI has made some temporary lamination plates from stainless steel that can be used until the copper plates are received. The delivery time on the tooling ranges from 3 to 6 weeks, depending on the tool.

Summary

In general, the progress on this program to date has been very good and within the established scheduled times. The DLI furnace has been turned on, the glazing, and oxidizing profiles have been set up, and DLI has verified that they produce good results. The DLI plating line is operational, and copper test sheets have been used to establish the initial cleaning and plating processes. The AMI printer, while not yet in, is on schedule for delivery. Meanwhile, artwork has been generated for basic print patterns and screens have been ordered. Two experimental lots of tape have been cast by Mistler, and one lot was evaluated. Cermalloy has made the first lot of thick film materials, and visually they look good. All materials are in except the Sem-Com glasses and they are due to ship on 9/4/96.

D. PLAN FOR NEXT QUARTER

- Conduct 2-sided substrate training sessions at Sarnoff
- Complete equipment set-up and checkout at DLI
- Verify that green tape supplied by Mistler is acceptable
- Verify that inks supplied by Cermalloy are acceptable
- Implement all major process blocks at DLI
- DLI to begin delivery of test structures to Sarnoff

Section II
WBS Task 2.2: Customize LTCC-M for Specific Applications

A. TASK OBJECTIVE

Extend the LTCC-M technology to meet any requirements of the technology demonstration modules, and any general packaging trends of the electronics industry.

B. INTRODUCTION

Progress is reported for the extension of LTCC-M to higher density circuits. To increase the circuit density of LTCC-M substrates, thick film inks have been developed that can produce test structures having 4 mil diameter vias and 4 mil lines and spaces.

C. HIGH DENSITY CONDUCTOR PATTERNS

Background:

Fine line-width conductors and spaces are essential for high density MCMs. For manufacturability of low cost MCM-Cs with such high density of interconnects, lines and spaces in particular, it is necessary that the screen printing process be continuous without interruptions in order to increase throughput. However, owing to the nature of printing fine lines, screens with fine intricate patterns get clogged during the printing operation due to various reasons, such as drying of the ink, introduction of unduly large particulates into the ink, etc. To counter this problem, manufacturers of screen printers allow for a 'swipe' cleaning of the screens after every 10 printing passes or so, such that the throughput remains high and at the same time clogging of the screens can be avoided.

Objective:

- Develop a simple, robust, cost effective, and manufacturable process for successful repeated screening of fine lines and spaces (a minimum of 4 mil wide lines and 4 mil space between them) of conductor lines for the LTCC-M based high density MCM-Cs.
- Demonstrate the reliability of test structures having 4 mil lines, spaces, and vias.

Major problems to solve:

- Formulate inks that will reduce fast drying of the inks on the intricate patterns on the screen and also prevent clogging of the screens.
- Optimize the conductor printing process such that at least 10 screen printing passes can be made before the screen needs cleaning.

Approaches to solve the problems:

A large number of experiments were designed to tackle the above mentioned problems. To begin with, a new test pattern was designed which concentrated on the fine line-width and space conductor printing. This pattern involved twenty pairs of each of 6 mil., 4 mil., 3 mil., and 2 mil. lines and spaces with a gap of 0.125"

between each set. These lines were at least 2.0" long and had probe pads at the very end of the lines, to test for continuity after co-firing.

It is believed that this pattern is necessary in addition to the high density test patterns mentioned in previous reports to meet the objective of this task. A new type of screen was purchased for this task which involved a finer mesh of 400, a finer wire diameter, finer emulsion and a calendered pattern for the mesh. This pattern will now on be referred to as 6432 pattern. The other two patterns, 290-L1 and 290-L3 are from the high density test patterns that used special alloy 290 mesh screens as mentioned in previous reports.

Ink formulation is considered to be the major task in achieving the goals of the objective. As a start, the top conductor ink, which was able to print two to five passes before clogging in 290-L1 pattern, was used. This ink was not able to print more than two passes before clogging; this negative result was thought to be caused by the use of silver flakes and larger particle size of the added glass powders. Several inks were then formulated with varying particle sizes of glass, and inorganics to organic carrier ratio. The organics used were a combination of resins VC-1 and VC-2 and the added solvents and surfactants were butyl carbitol and lecithin respectively; precise formulations of these organics are mentioned in previous reports. The results are tabulated in Table II.1. Note that the results indicated are for the twenty pairs of 4 mil. lines and 4 mil. spaces of the 6432 pattern.

Summary of Printing Results:

It is noted that the best screen printing results were obtained for the ink (FLS-14) which had a finer particle size of the added glass, had no silver flakes and had an inorganic to organic ratio of 71:29 on a weight basis.

Table II.1

INK ID	Ag:Glass (wt. basis)	Glass Particle Size (μm)	Inorganic: Organic (wt. basis)	Results (# prints before clog in 4 mil. line)
FLS-0	0 g of glass	-	77:23	5, on 6432 pattern
FLS-1	75:25	2.3	77:23	7, on 6432 pattern
FLS-2	75:25	4.8	77:23	4, on 6432 pattern
FLS-3	75:25	10.5	77:23	3, on 6432 pattern
FLS-4	75:25	2.3	48:52	7, on 6432 pattern (shorted)
FLS-5	75:25	4.8	48:52	3, on 6432 pattern (shorted)
FLS-6	75:25	10.5	48:52	3, on 6432 pattern (shorted)
FLS-7	75:25	2.3	79:21	9, on 6432 pattern
FLS-8	75:25	2.3	81:19	7, on 6432 pattern
FLS-9	75:25	2.3	83:17	7, on 6432 pattern
FLS-10	75:25	2.3	85:15	5, on 6432 pattern
FLS-11	75:25	2.3	75:25	9 each on 6432 & 290-L1 patterns
FLS-12	75:25	2.3	74:26	7 on 6432 & 9 on 290-L1 patterns
FLS-13	75:25	2.3	72:28	11 on 6432 & 12 on 290-L1 patterns
FLS-14	75:25	2.3	71:29	12 each on 6432 & 290-L1 patterns
FLS-15	75:25	2.3	69:31	9 each on 6432 & 290-L1 patterns
FLS-13.5	75:25	2.3	71.5:28.5	10 each on 6432 & 290-L1 patterns
FLS-14.5	75:25	2.3	70:30	10 each on 6432 & 290-L1 patterns
FLS-15.5	75:25	2.3	68.5:31.5	7 each on 6432 & 290-L1 patterns

High Density Test Board Reliability Studies:

Two additional sets of high density test boards (4-layer boards with 9 daisy chains interconnecting a total of 978 vias; 4 mil diameter vias and 4-5 mil wide lines) were fabricated using green tape punched with 4 mil diameter holes and with the following materials: ABT-60 green tape; INJ-202B via ink; KMB-21D buried conductor ink and TC-9 top conductor ink. The high density via patterns were injection filled. The buried conductor ink used here is comprised solely of Ag powder Q and resulted in improved printability of the fine line traces relative to the mixed Ag flake/Q powder inks used previously. Although the fired parts still had some defects associated with imperfect printing, the percentage of complete daisy chains was much higher than with the previously fabricated parts. None of the parts had >10 opens.

Five parts from this group were subjected to temperature cycling (-55 to +125°C, 30 min. holds at temperature) and five parts were subjected to 150°C temperature aging; the resistances of the daisy chains were monitored as a function of test cycles or hours. A summary of the test parts and total test cycles or hours that each part underwent is given in Table II.2. No significant variations in chain resistance were observed in parts tested for >600 temperature cycles and aged for up to 1800 hours at 150°C. Typical results for temperature cycling and temperature aging tests are shown graphically in Figures II.1 and II.2. In the this test pattern, chain #s 1-3 are high density chains (4 mil diameter vias on 16 mil centers with (1) 4 mil wide line between vias; 120 vias per chain); chain #s 4-6 are medium density chains (4 mil diameter vias on 30 mil centers with (2) 5 mil wide lines with 5 mil spaces between vias; 120 vias per chain); and chain #s 7-9 are low density chains (4 mil diameter vias on 42 mil centers with (3) 5 mil wide lines with 5 mil spaces between vias; 84 vias/chain).

Table II.2: **Reliability Test Part Summary**

Part ID	Test	Total Test Cycles (-55 to +125°C)	Total Test Hours (150°C)
C1	Temp. Cycling	626	
C5	Temp. Cycling	626	
C6	Temp. Cycling	570	
D1	Temp. Cycling	595	
D3	Temp. Cycling	565	
C3	150°C Temp. Aging		1818
C4	150°C Temp. Aging		1818
C2	150°C Temp. Aging		1818
D2	150°C Temp. Aging		1727
D4	150°C Temp. Aging		1651

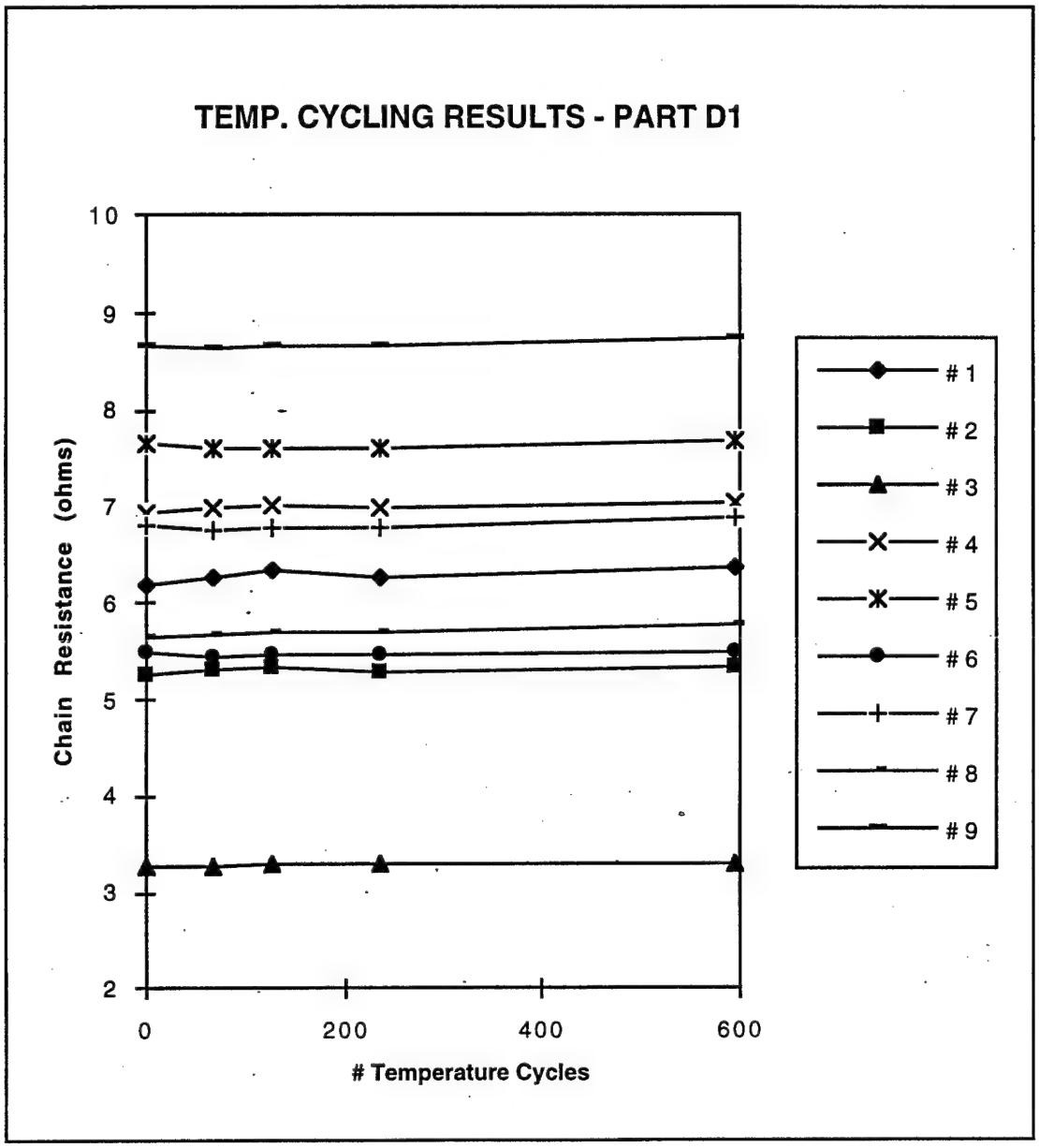

Figure II.1: Typical thermal cycling (-55 to +125°C) data for a daisy chain test specimen.

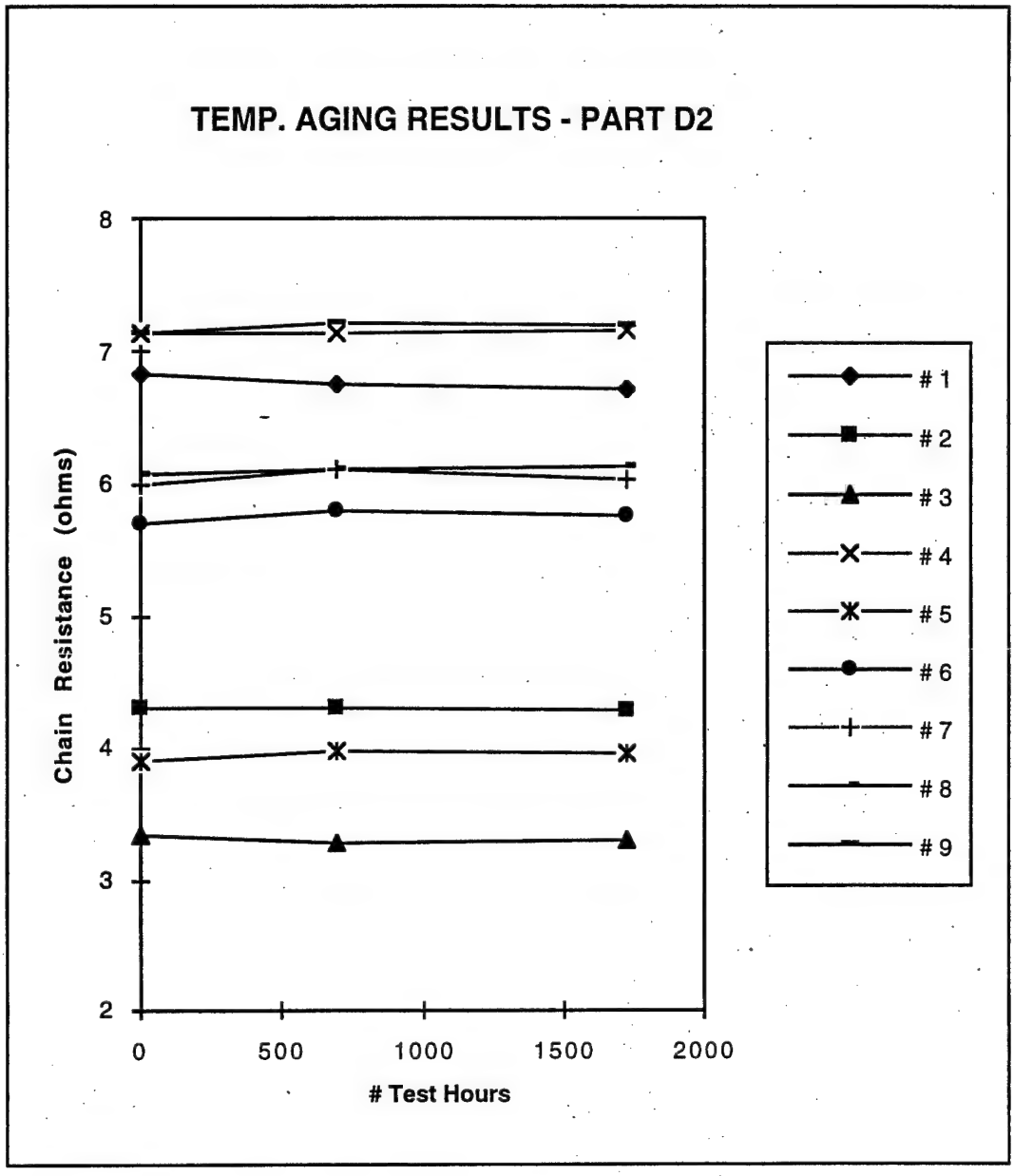

Figure II.2: Typical thermal aging (150°C) data for a daisy chain test specimen.

D. PLAN FOR NEXT QUARTER

- Formulate conductor inks using solvents that have much lower vapor pressures at room temperature
- Begin reliability testing of 4 mil test structures made with the better printing ink formulations
- Continue reliability testing of Ag and AgPd thick film top conductors
- Begin fabrication of a BGA package by combining results of the LTCC-M Customization Tasks

Section III
WBS Task 2.3: Fabrication and Testing of Technology Demonstration Modules

A. TASK OBJECTIVE

The objective of this task is to design, fabricate, assemble, and test 4 different technology demonstration modules. These modules are: (1) an optoelectronic transceiver module, (2) a power amplifier package, (3) an advanced PCMCIA card, and (4) a Power Electronic Building Block (PEBB).

B. INTRODUCTION

The four technology demonstration vehicles planned for this program were chosen because each module had clear military applicability, and also met the requirements of the consumer marketplace. Table III.1 shows the application of each demonstration module to the needs of the US armed forces.

Table III.1:
Military Relevance of LTCC-M Technology Demonstration Vehicles

Prototype Application	Supporting Co.	Type	Military Relevance
Advanced PCMCIA Card (ORBCOMM Modem)	Torrey Science	Mixed Signal Module	1. Similar electronics needed for global tracking of high value and critical military materials and components (e.g. armaments) 2. Supports DoD: • Materials Command • Logistics Command • Transportation Command • "Total Asset Visibility" program 3. Technology applicable to the following: • NSA (R2) dual function PCMCIA card • Trackers • Message Terminals • CESEL • Special Forces replacement of high frequency radio systems (miniaturization) • Global extension of communications in Force 21 "Digital Battlefield" 4. Applies to Military Global Mobile Information Systems
High Power Motor Controller (Power Electronics Building Blocks)	Harris	High Power Single Chip Package	1. Supports US Navy Contract # N-00024-94-C-4088 (an Advanced Tech. Demo. with Naval Sea Systems Command) 2. Computer controlled Integrated Variable Speed Electric drive for ships (surface and subsurface) and tanks 3. Computer controlled Electric Actuators for airplanes, ships, and tanks 4. Auxilliary Power Unit Generators, Solid State Power Controllers for airplanes 5. Power Inverters and Converters for ships and airplanes
Optoelectronic Transceiver Module	AMP	MCM	1. Supports the construction of low cost broadband networks at military bases and installations. 2. Such networks support: • ATM based switching architectures • Transfer of large amounts of graphical and multimedia data • Digital signals • Encrypted signals 3. Supports ARPA contract "Manufacturable Low Cost Single-Mode Bi-directional Links for Fiber in the Loop Optical Networks" • Currently LTCC-M is the sole technology for this application
Power Amplifier Packages (microwave)	Raytheon	GaAs single chip package	1. Portable government cellular communications systems and wireless LANs 2. Applies to Military Global Mobile Information Systems

C. OPTOELECTRONIC TRANSCEIVER MODULE

Under this program Sarnoff, and AMP will develop a package that will integrate an optoelectronic MCM, an optical fiber, several silicon devices, and several passive components. This program provided tested bare-board LTCC-M packages to AMP (for module assembly) in May, 1996.

To meet the various design configurations of AMP, two similar packages were designed and fabricated together in a multi-up format. The decision to fabricate the "A" and "B" designs together minimizes the overall NRE costs for building this package.

1. Challenges of this package

- Use of large area solid ground planes and shielding structures on all layers for noise immunity
- Crosstalk minimization
- Need for high precision cavities to minimize bond wire length of the high speed interconnections, especially the 1.2 GBit/sec link
- Need for a high thermal conductivity base for laser stability and thermal management
- Package must be hermetic

2. Package Statistics

Size: 0.54" x 1.10"
Components interconnected: Optoelectronic MCM, 2 bare ASICs (Si), resistors and capacitors
Interconnect density: general design with 8 mil lines/spaces and 8 mil diameter vias; 6 mil lines and spaces in the bond pad areas.
Number of layers: 3
Number of vias: 258
Number of component mounting cavities: 2
Number of nets: 26

3. Module Fabrication

In May 1996 thirty (30) packages were delivered to AMP for module assembly and testing. Details of the package fabrication were provided in the 6/14/96 Quarterly Report. These modules were designed for use with 2 mm square ASICs. However, the die that were delivered to AMP (under a separate DARPA program) were too large (and out of spec.). Cutting these custom ASICs to size has delayed the module assembly and testing phase of this program.

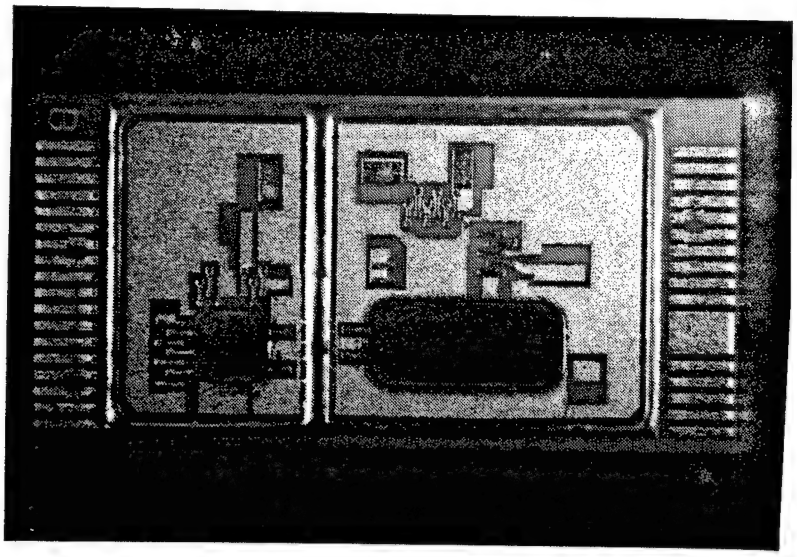

Figure III.1: An optical transceiver package (0.54" x 1.1") fabricated using LTCC-M substrate technology.

D. POWER AMPLIFIER PACKAGE

The objective of this task is to design, fabricate, assemble and test a low cost power amplifier package for a GaAs microwave device. The package will be designed, assembled and tested by Raytheon and fabricated by Sarnoff.

1. Challenges of this package

- Low loss microwave package for operation at C-Band frequencies
- Integral metal base to minimize "moding" effects
- Need for high precision, tiered cavities to minimize bond wire lengths from die to package
- Need for a high thermal conductivity base for 10 W power dissipation
- Thermal expansion match to GaAs for solder attachment of bare die to metal base
- Low loss transmission lines through seal rings

2. Package Assembly and Evaluation

As part of its evaluation of the suitability of LTCC-M to microwave packaging, Raytheon has designed an LTCC-M package for its PA92 power amplifier. Last quarter, bare substrates were delivered to Raytheon. This past quarter, the substrates were assembled and evaluation was begun by Raytheon. As shown in Figure III.2, each package contained a bare GaAs die and 18 surface mount capacitors. Within an accurately sized cavity in the ceramic, The GaAs die was eutectically soldered to the Cu/Mo/Cu metal base. The PA92 consists of two electrically independent power amplifiers in a mirror imaged layout. The two amplifiers are connected together on chip in operation, and are matched to a 25Ω

source and load impedance at the RF input and output ports. The PA92 meets the following requirements:

Parameter	Performance
Frequency	C-Band
Output Power	≥ 38dBm
Gain	≥ 27dB
Efficiency	≥ 40%

In order to match the amplifier to 50Ω, a one stage quarter transformer was designed into the package at both the chip's input and output. In order to measure the insertion loss and return loss of the package itself, without the chip, two 50Ω lines were epoxied in parallel inside the chip cavity in place of the chip. Three wirebonds were connected to both sides of each 50Ω line. Typical insertion loss and return loss are shown in Figures III.3(a) and (b) respectively. In the region of operational interest, the return loss is less than -13.8 dB and the insertion loss is between -0.58 and -0.83dB. This data is good for a package of this size. The measured data includes effects of transmission lines epoxied inside the package cavity, the wirebonds, and the fixture connectors. The null in the package's insertion loss response between 3.9 GHz and 5.5 GHz is attributed to the inductance of the wirebonds.

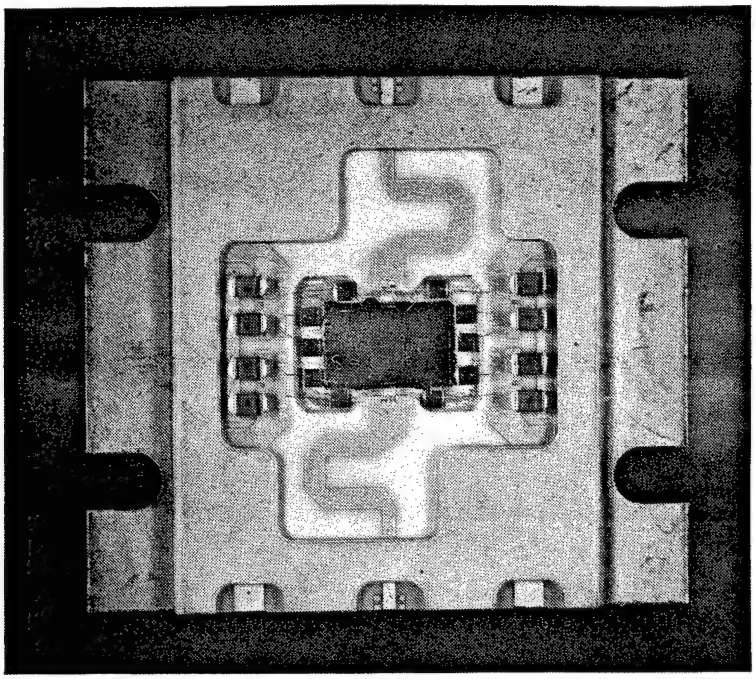

Figure II.2: An assembled C-Band Power Amplifier module fabricated on an LTCC-M substrate.

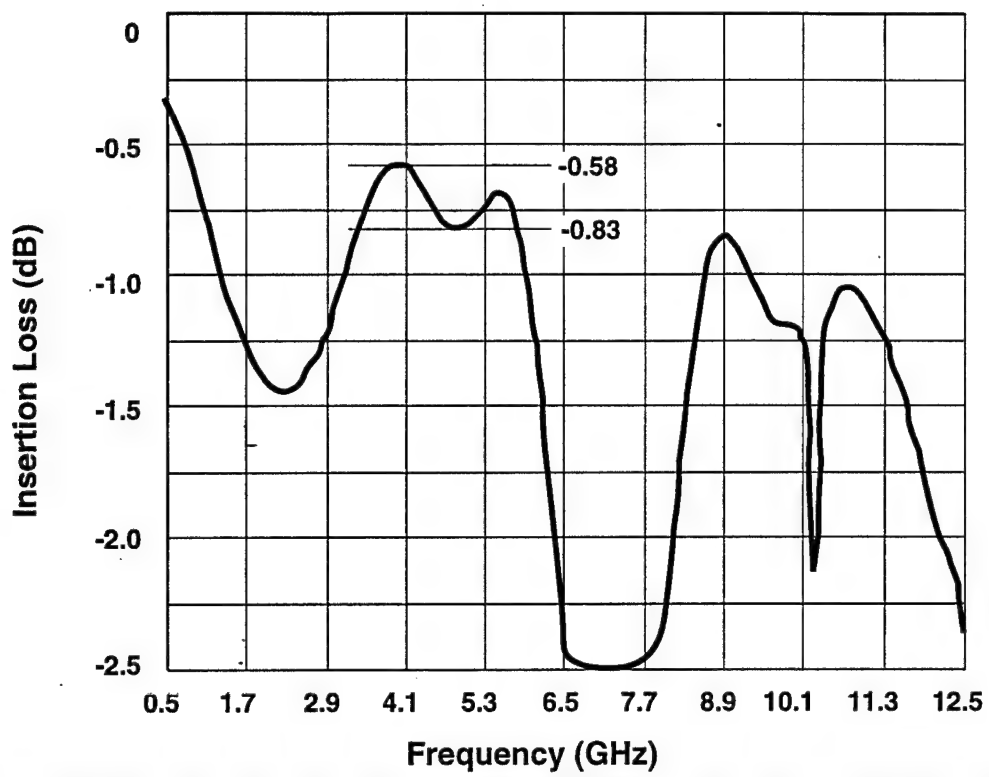

Figure III.3(a): Insertion loss response of the LTCC-M C-Band Power Amplifier package.

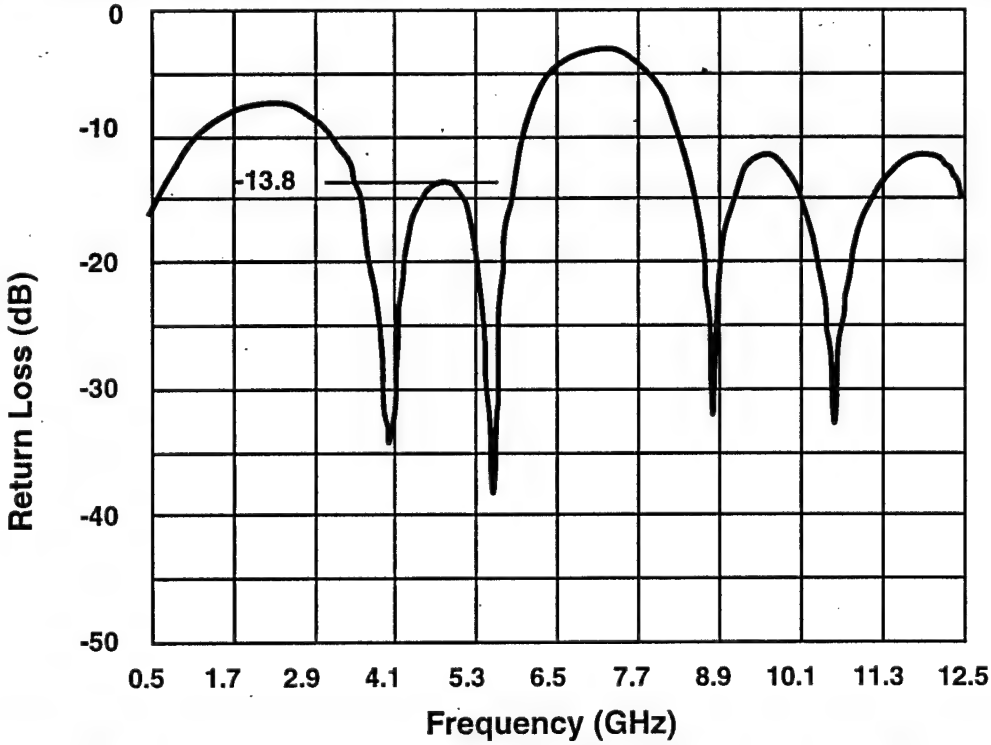

Figure III.3(b): Return loss response of the LTCC-M C-band Power Amplifier package.

Initial testing of the packages with the PA92 chip in place has begun. Figure III.4 shows the results of tests made on the fully assembled amplifier in the LTCC-M package. The package is capable of handling 38 dBm of output power at efficiencies greater than 45%.

This package has met all specifications; and a key reason for this was the integration of the impedence matching transformers in the substrate. Raytheon is pleased with the performance of this LTCC-M package. Future Raytheon plans for LTCC-M include the demonstration of its applicability for products that operate millimeter wave frequencies.

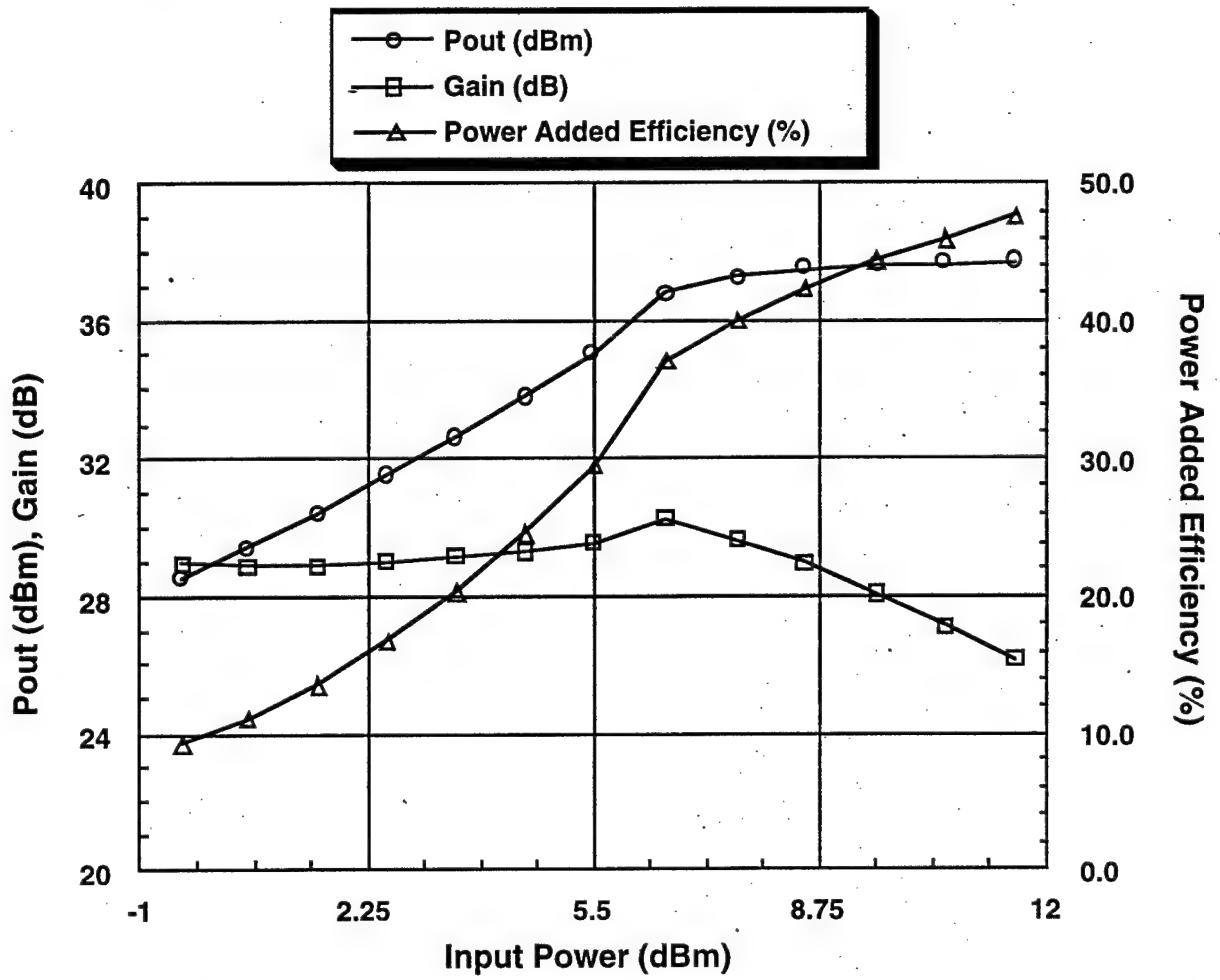

Figure III.4: Performance of a fully assembled C-Band power amplifier in LTCC-M package.

E. ADVANCED PCMCIA CARDS

Design:

Torrey Science has completed the design of the RF Modem Module and has sent the circuit layout data to Sarnoff for substrate fabrication. Some key features of the design are:

- The design is based on an extended PCMCIA Type II card format.
- This is a 2-sided module with digital circuitry on one side of the LTCC-M substrate and the RF circuitry on the other side.
- Interconnections between the digital and RF circuitry are provided by means of insulated feedthroughs in the Cu/Mo/Cu metal core.
- Interconnections within the digital circuitry are provided by means of a 6-layer multilayer construction. The RF side consists of four ceramic layers.
- The design utilizes entirely surface mount devices and packages, bare dies (total of 16), and surface mount connectors for external connections.

The device outlines and surface metallization for each side, and the feedthrough holes in the metal core are schematically represented in Figures III.5 through III.9

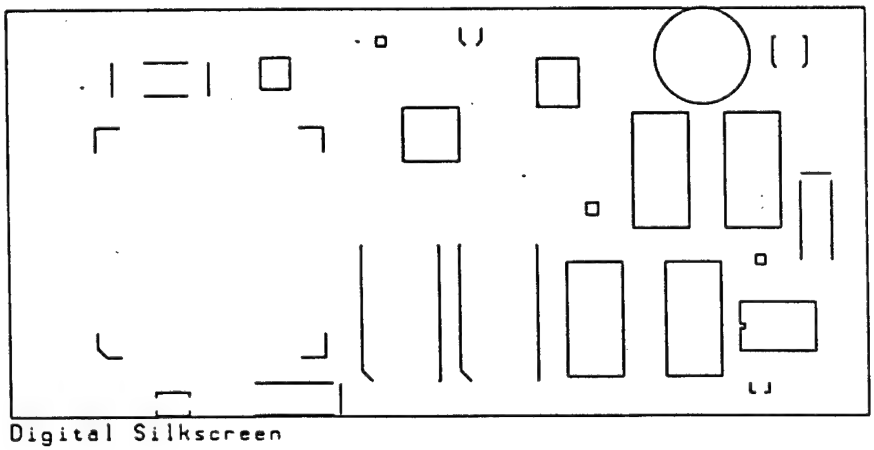

Figure III.5: *Outline of major devices on the digital side.*

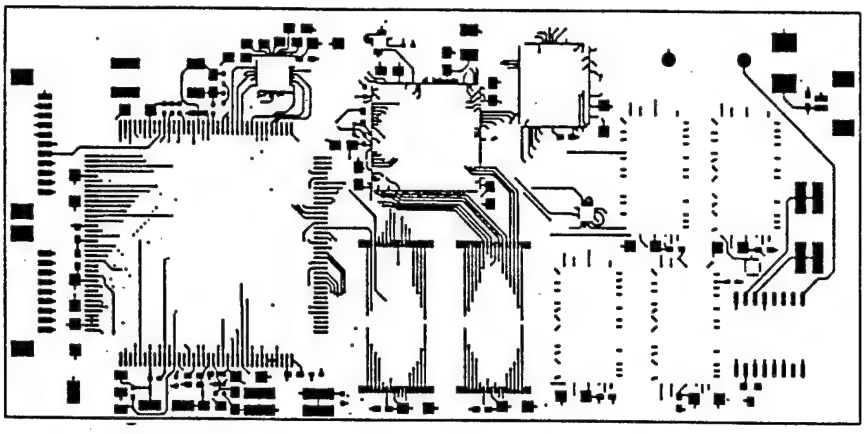

Figure III.6: *Digital side top surface metallization including interconnects, solder pads, and bonding pads.*

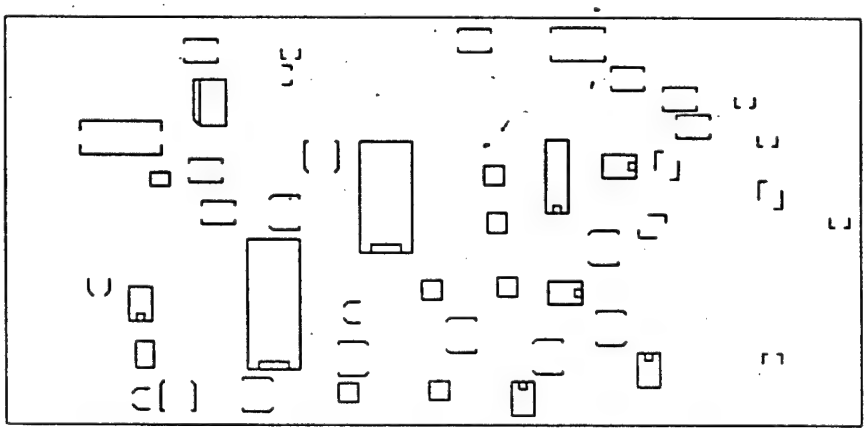

Figure III.7: *Outline of major devices on the RF side.*

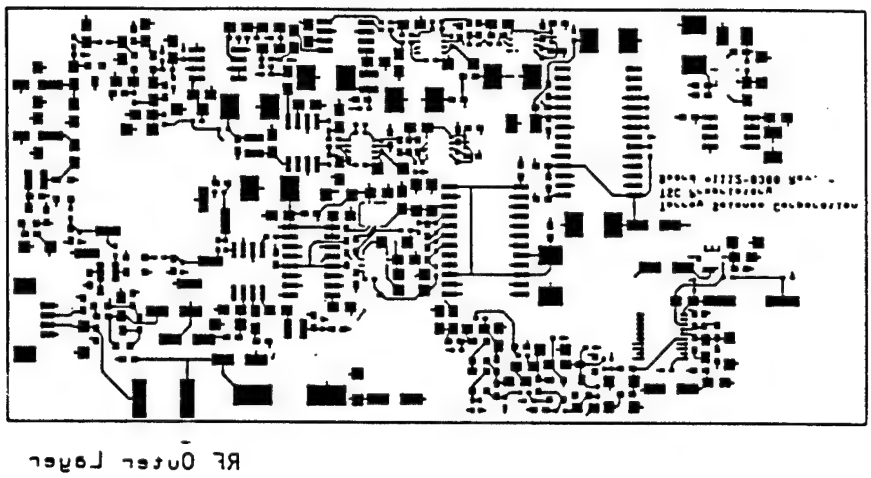

Figure III.8: *RF side top surface metallization including interconnects, solder pads, and bonding pads.*

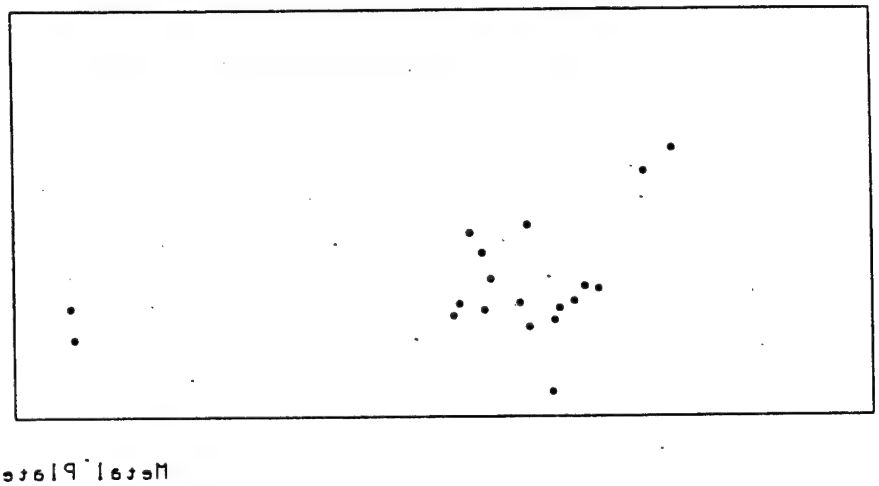

Figure III.9: *Outline of metal core and feedthrough locations.*

Substrate Fabrication:

Design data from Torrey Science are being converted to various fabrication tools at Sarnoff:

- Via punch files have been supplied to the tool and die vendor for building dedicated tooling for punching vias in the ceramic tape. A total of five die sets consisting of a blanking die, two via punch dies for the digital side, and two via dies for the RF side have been ordered.
- Gerber files of the various layers of circuitry with alignment keys are being supplied to printing screen and stencil suppliers.
- Additional layers of artwork (that are not part of the Torrey Science design package) needed for LTCC-M construction, such as glaze layers,

contact metal pads layers, and stabilization layers will also be supplied to the screen vendor.

- Substrate fabrication will begin as soon as the die sets, screens, and stencils are received.

Module Assembly:

Torrey Science has selected CTM, Microelectronic Packaging, Inc. as the module assembler. Several steps are being taken to facilitate the assembly process:

- Double-sided solder assembly trials were run at Sarnoff to verify materials-process compatibility. Good results were obtained with eutectic Sn-Ag as the high temperature solder and eutectic Sn-Pb as the low-temperature solder. These test modules were subjected to 125 of -65/+150°C thermal cycles and passed continuity tests and visual criteria.
- Enhancements to top surface conductor have been incorporated for better reliability.
- Double-sided substrates with only top surface metallization will be fabricated and provided to CTM by mid-September for initial trials and process development.

Issues:

Two factors have caused considerable delay in this part of the program making the remainder of the schedule very tight:

1. Difficulties in the procurement of needed components, especially bare dies, led to delays in completing the design by Torrey Science.
2. Design software differences between Torrey Science and Sarnoff have led to delays in procuring substrate fabrication tools at Sarnoff.

Both issues have been resolved and intensive effort is being put into speeding up the remaining tasks so that the program goals can be achieved successfully and on time.

F. POWER ELECTRONIC BUILDING BLOCKS (PEBB)

1. Background

The objective of this task is to design, fabricate, assemble and test a low cost, PEBB "lid" in support of the U.S. Navy PEBB program, and to meet the packaging needs of high current semiconductor devices. PEBB "lids" are high power device substrates that connect the power device to its control signals on a printed wiring board, and also are part of the thermal management system that draws the heat away from the device (and the printed wiring board). This package will eliminate the need for traditional wirebonding for contact formation with external electrodes. This is also a significant improvement over the currently available plastic based power modules that have high parasitic inductance and resistance losses associated with wirebonding. In addition, reliability concerns regarding fatigue of bond wires

and fracture of brittle semiconductor die under the stresses of the wirebonding process are also eliminated. The total device size is also reduced. The "lid" package will be designed, assembled and tested by Harris Power R & D and fabricated by Sarnoff.

2. Package Challenges

- Prevent camber in the LTCC-M board after co-firing with 0.005" Cu-Mo-Cu metal core and six layers of glass ceramic tape.
- Accommodate very high density of vias over a large portion of the LTCC-M board, resulting from inherent design and multi-up of parts in a single board.
- Achieve good via contact through six layers of glass ceramic tape down to the metal core.
- Prevent cracking of the glass ceramic and cracks in the via material itself throughout the entire LTCC-M board.
- Devise and optimize the process for patterning the 0.005" Cu-Mo-Cu metal core by etching.

3. Module Fabrication

Details of the PEBB package fabrication were provided in the 6/14/96 Quarterly Report. This past quarter, the remainder of the order for 200 packages were tested and delivered to Harris for module assembly and evaluation. A sample package is shown in Figure III.10. These packages are currently being assembled into PEBB "lids" by Harris.

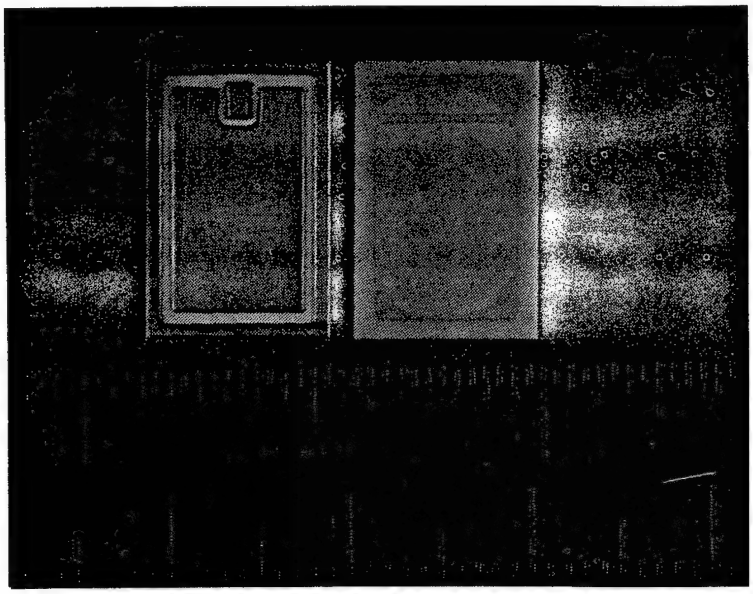

Figure III.10: Two PEBB package prototypes showing the metal patterns.

G. PLAN FOR NEXT QUARTER

Optoelectronic Transceiver Module:

- AMP to procure properly sized ASICs
- Module assembly by AMP
- Module evaluation by AMP

Power Amplifier Package:

- Module assembly and evaluation completed

Advanced PCMCIA Cards:

- Complete LTCC-M layout
- Complete tool and screen making
- Complete substrate fabrication
- Complete assembly trial runs

Power Electronic Building Blocks:

- Module assembly by Harris
- Module evaluation by Harris

Section IV
Important Findings

A. TECHNOLOGY TRANSFER TO MERCHANT SUPPLIERS

- The LTCC-M technology transfer to Dielectric Laboratories Inc. (DLI) began in July, 1996. All training sessions for the processes required for fabricating the technology demonstration vehicle (C-band Power Amplifier Package) have been completed.
- First green tape casts of ABT-52 SC have been delivered to DLI by R.E. Mistler, Inc. Evaluation has begun.
- First lot of thick film inks have been delivered to DLI by Cermalloy. Evaluation has begun.
- The belt furnace has been received and installed at DLI. All required furnace profiles are being established.
- The Ni plating line is running at DLI. The initial set of plated parts is being evaluated.

B. CUSTOMIZE LTCC-M FOR SPECIFIC APPLICATIONS

- Developed ink formulations that shown better screen printing characteristics for lines between 2 and 5 mils wide, and maintain their printing characteristics for longer printing sessions.
- Accelerated aging tests for high density conductors having 4 mil lines, spaces and vias do not show any signs of deterioration after more than 1600 hours of storage at 150°C, and after more than 560 thermal cycles between -55°C and +125°C.

C. FABRICATION AND TESTING OF TECHNOLOGY DEMONSTRATION MODULES

- The C-Band Power Amplifier met all specifications; and a key reason for this was the integration of the impedence matching transformers in the substrate.
- Completed assembly of C-band Power Amplifier packages at Raytheon. Acceptable power output has been demonstrated. Testing over the operational region showed insertion loss between -0.58 and -0.83dB, and return loss less than -13.8 dB. This data is quite good for a package this large.
- The C-Band Power Amplifier is capable of handling 38 dBm of output power at efficiencies greater than 45%.
- Delivered the remainder of the order for 200 PEBB "lids" to Harris for module assembly.
- Torrey Science has obtained commitments from bare die suppliers so that the RF Modem Module, designed as a Type 2 PCMCIA card will contain 16 bare die.
- Torrey Science has completed the design of the RF Modem Module.
- Design software differences between that used at Torrey Science and at Sarnoff have been overcome so that hard tooling and printing screens have been ordered.

Section V
Significant Developments

Dielectric Laboratories Inc. (Cazenovia, NY) will replace Alcoa Electronic Packaging as Sarnoff's LTCC-M Technology Transfer partner. An expedited schedule will be employed to complete this transfer by January 15, 1997. It is expected that Dielectric Laboratories will be a merchant supplier of LTCC-M packages and substrates to both commercial and military end-users.

Section VI
Plan for Further Research

TECHNOLOGY TRANSFER TO DIELECTRIC LABORATORIES INC.

- Conduct 2-sided substrate training sessions at Sarnoff
- Complete equipment set-up and checkout at DLI
- Verify that green tape supplied by Mistler is acceptable
- Verify that inks supplied by Cermalloy are acceptable
- Implement all major process blocks at DLI
- DLI to begin delivery of test structures to Sarnoff

CUSTOMIZE LTCC-M FOR SPECIFIC APPLICATIONS

- Formulate conductor inks using solvents that have much lower vapor pressures at room temperature
- Begin reliability testing of 4 mil test structures made with the better printing ink formulations
- Continue reliability testing of Ag and AgPd thick film top conductors
- Begin fabrication of a BGA package by combining results of the LTCC-M Customization Tasks

FABRICATION AND TESTING OF TECHNOLOGY DEMONSTRATION MODULES

Optoelectronic Transceiver Module:

- AMP to procure properly sized ASICs
- Module assembly by AMP
- Module evaluation by AMP

Power Amplifier Package:

- Module assembly and evaluation completed

Advanced PCMCIA Cards:

- Complete LTCC-M layout
- Complete tool and screen making
- Complete substrate fabrication
- Complete assembly trial runs

Power Electronic Building Blocks:

- Module assembly by Harris
- Module evaluation by Harris

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The quarterly progress for the Ceramic/Metal Composite Circuit-Board-Level Technology for Application Specific Electronic Modules is described in this report. Data is reported for the following tasks: Technology Transfer to Merchant Suppliers, Customize LTCC-M for Specific Applications, and Fabrication and Testing of Technology Demonstration Modules.

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